1050™ DISK DRIVE FIELD SERVICE MANUAL

Revision 1.0
by jer
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SECTION 1

THEORY OF OPERATION

OVERVIEW

The ATARI 1050 Disk Drive is a record/playback device that allows information to be stored and retrieved quickly and accurately. The actual recording is much like a tape recording process and is done on similar material. The data is magnetically recorded on a 5.25 inch diameter diskette. Each diskette can store 88K bytes of data in single density mode and 133K bytes in double density, however double density can only be implemented in conjunction with DOS 3. The diskette is inserted through a door in the front panel of the drive unit. The 1050 Disk Drive is used with a single ATARI 400, 800 or 1200 Computer with a minimum of 16K of RAM installed.

Figure 1 is a simplified block diagram of the functional flow of the 1050 follows. Each of its functional units are explained in greater detail below.

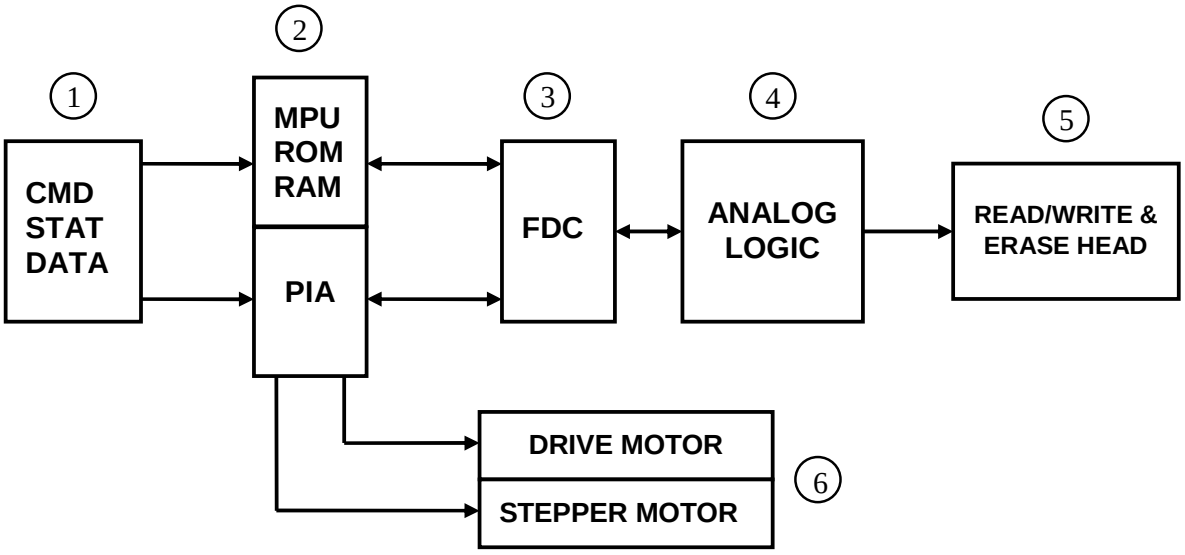


Figure 1. Simplified Block Diagram

Block 1 Includes the Data Input/Output (I/O) connectors. They are the origin and destination of all commands, status and data.

Block 2 Includes the Microprocessor(MPU), Read-Only-Memory (ROM), Random Access Memory (RAM) and Peripheral Interfaces Adaptor (PIA). They process all commands and control data flow to and from the console.

Block 3 Includes the 2793 Floppy Disk Controller (FDC). The FDC controls data flow to and from the diskette.

Block 4 Includes the Analog Logic. The Analog Logic processes all data to and from the Read/Write Head.

Block 5 Includes the Read/Write and Erase Head.

Block 6 Includes the Drive Motor and Stepper Motor which are located in the Drive Mechanism. They receive signals from PIA.

OPERATOR FUNCTIONS

Each 1050 Disk Drive comes with an AC Power Adaptor and a Data Cord. Figure 1-2 shows how to connect the Disk Drive and computer console.

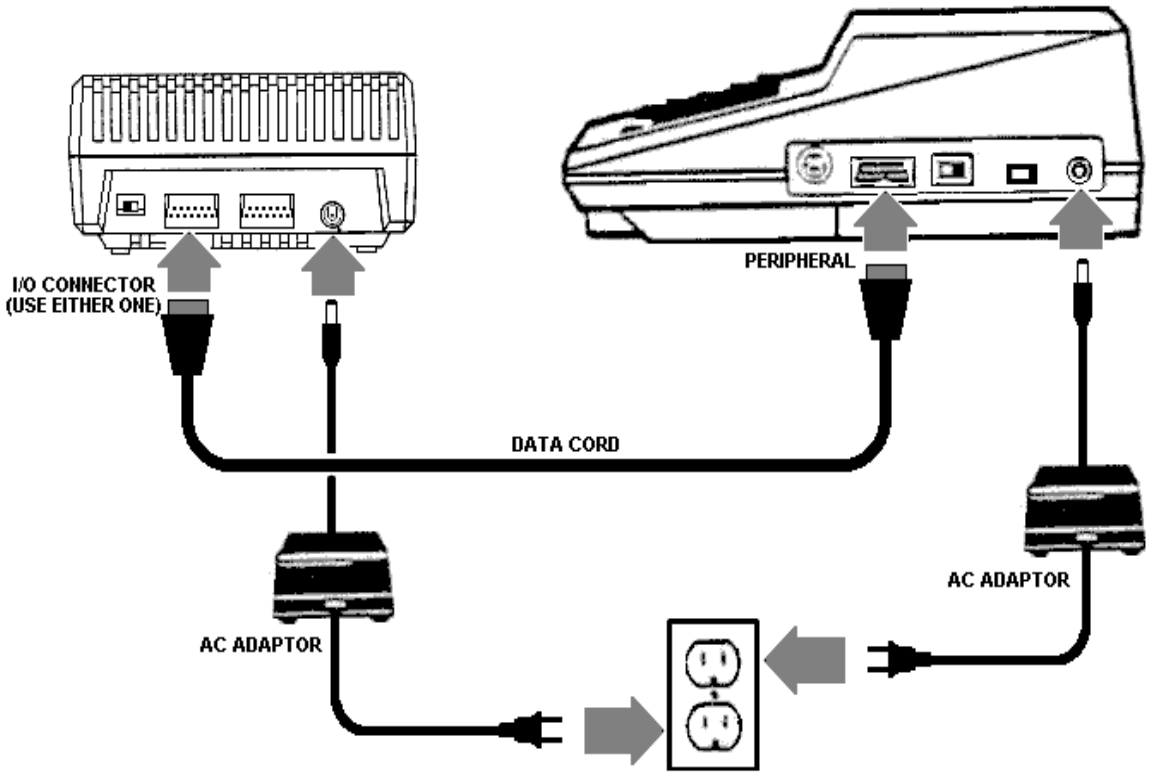


Figure 2. System Hook-up

The Controls/Indicators are located on the front and back panels of the 1050. The front panel of the 1050 contains the Activity Light, the Power Indicator Light, the Power ON/OFF switch, and the door latch. The rear panel of the 1050 contains the Input/Output (I/O) connectors, Power-Jack and Drive Code Switch. (Use Atari 810 switch settings to identify drive number 1,2,3 or 4).

These functions are illustrated in Figure 1-3 and discussed in the following paragraphs.

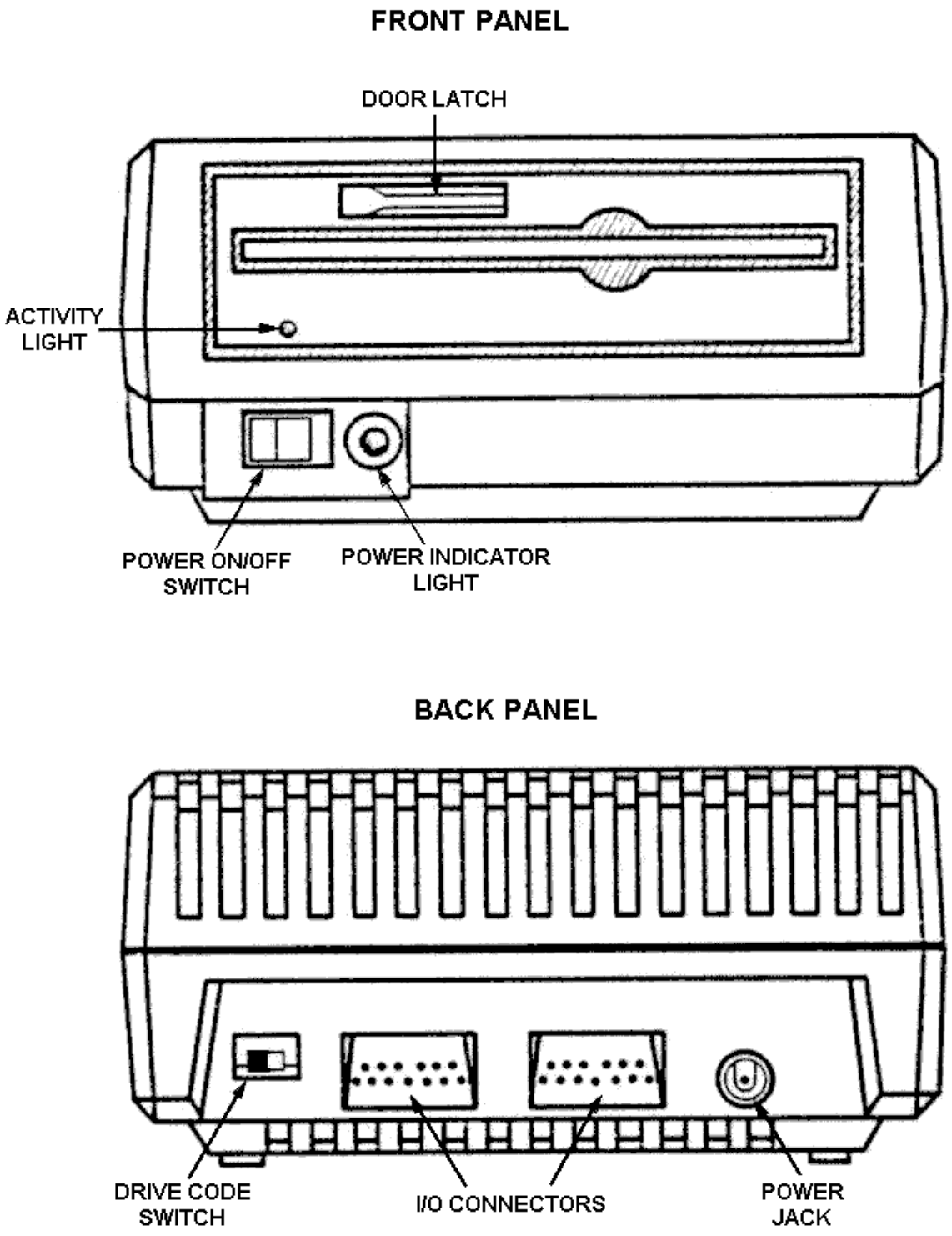


Figure 3. ATARI 1050 Disk Drive Control/Indicators

Front Panel

The Activity Light lights whenever the drive is reading from or writing to a diskette or when the diskette is first inserted, and the door latch turned down. DO NOT OPEN THE DRIVE DOOR, TURN POWER OFF, OR ATTEMPT TO REMOVE THE DISKEETTE WHEN THE LIGHT IS ON!

The Power Indicator lights whenever power to the Drive is ON.

The Power ON/OFF switch is a toggle switch pushed to the right for ON, and to the left for OFF. ALWAYS insert or remove diskette with Power ON.

The Door Latch turns down to close the door after a diskette is inserted. The Activity Light then lights for a few seconds. The latch turns parallel to the diskette slot for removing the diskette.

Back Panel

The Input Output (I/O) connectors are identical jacks for the data cords from the computer console or ether peripheral devices. Connections may be made in any other with either jack.

The Power Jack accepts the AC Power adaptor.

The Drive Code Switch is a 4 - position switch that tells the computer which drive it is communicating with.

Two switches (one black and one white are visible in the rectangular opening on the drive rear panel. Using a pen or screwdriver, move the switches to the correct position on each drive being used.
Drive Code Number Diagram shows the correct positions of the Drive Code Switch to set the identification of the Drive (1 thru 4).

MECHANICAL THEORY

The 1050 unit is compose on an outer case which houses the Driver Mechanism, Drive Motor, Head Carriage Assembly, Stepper Motor and PCB.

CASE

The 1050 outer case consists of three pieces of plastic.

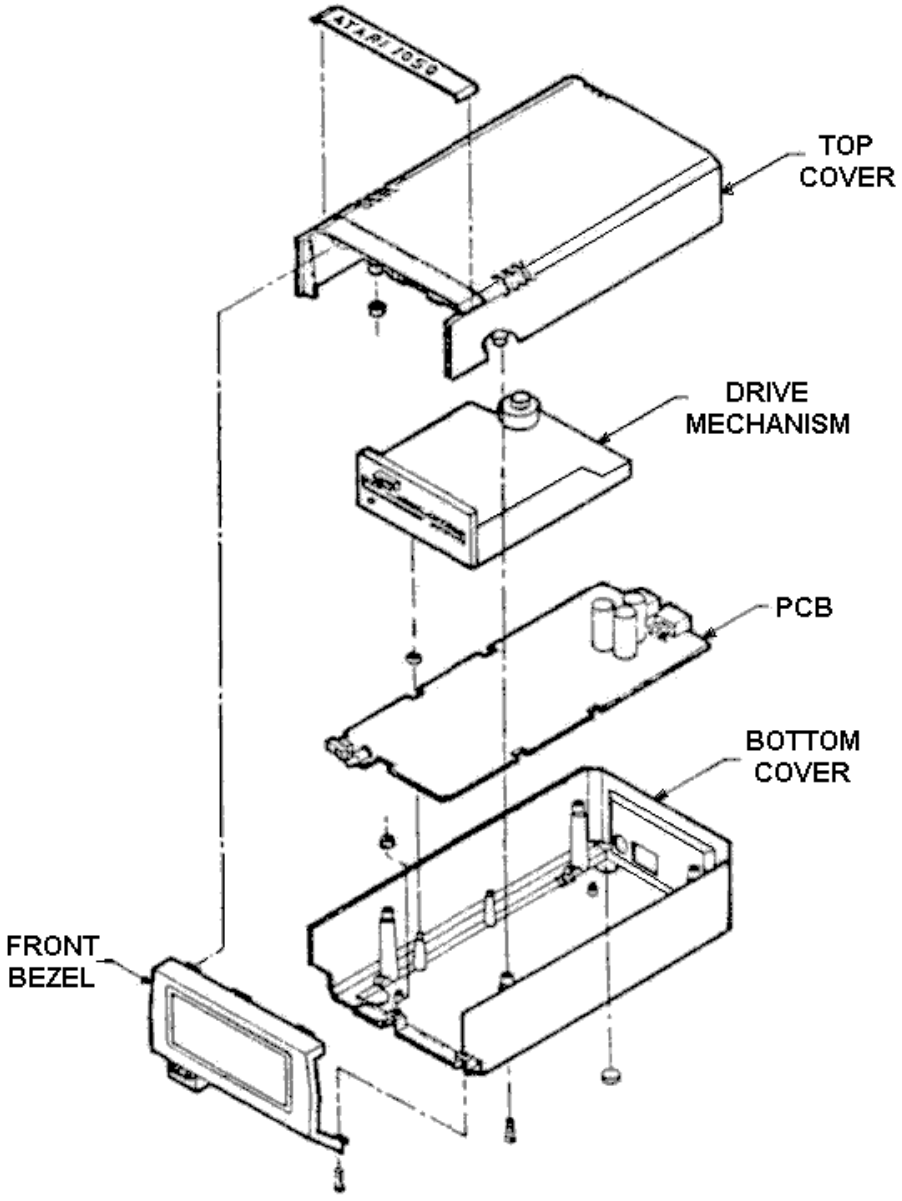


Figure 4. Exploded Diagram of the Disk Drive

Figure 1-4 illustrates the mechanical elements of the 1050 unit are discussed in the following paragraphs.

DRIVE MECHANISM

The Drive Mechanism provides mechanical and electronic linkage to the diskette. It is the physical assembly containing the Head Carriage Assembly, Drive Motor, Stepper Motor, and Write Protect sensor, Track 00 sensor, and Diskette Enable switch.

HEAD CARRIAGE ASSEMBLY

The Head Carriage assembly allows the head to be cycled across the diskette. It contains the Read/Write and Erase Head, the pressure pad and springy assembly.

DRIVE MOTOR

The Drive Motor is a DC motor which indirectly drives the diskette. It is attached by a drive belt to a flywheel which rotates the disk.

The DC motor includes an internal Tachometer, whose output is monitored in the Tach Feedback circuit. The Tach Feedback circuit senses changes in current and maintains a constant motor speed.

The activity Light (LED) comes on whenever the motor turns on.

STEPPER MOTOR

The Stepper Motor positions the head over a desired track. It is a four-phase motor. Each change in phase rotates the Stepper Motor shaft. This circular motion is converted to Linear motion by the positioning band/pulley assembly which links it to the head carriage.

The Stepper Logic is controlled by the PIA Chip. Four PIA, signals act as the Stepper Motor's four-phase inputs. These lines in various combinations, drive the Stepper Motor to reposition the Head Carriage Assembly from track to track.

PCB ASSEMBLY

All of the digital and analog logic for the 1050 is contained on one PCB.

POWER SUPPLY

The Power Supply provides the following voltages for use in the system:

- +5V DC regulated, which provided the voltage for the logic and for the 2793-02 Floppy Disk Controller,
- +12V DC (regulated), which feeds to Stepper Motor, Drive Motor, Zero Crossing Detector, Read/Write and Erase circuitry, and Tach feedback.

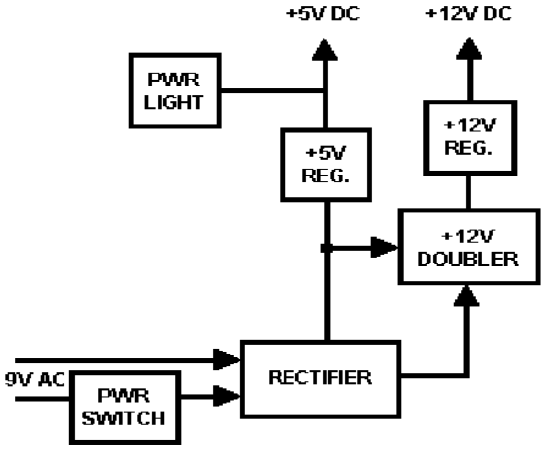


Figure 5. Power Supply Block Diagram

The 120V AC (or 230V AC) which comes into the system is stepped down to 9V AC by an external transformer (See figure 1-6).

The 9V AC is applied to the bridge rectifier on to PCB when the Power ON/OFF switch is turned ON. An internal 2A fuse in the adaptor provides current limiting protection.

POWER-UP LOGIC

The Disk Drive's Power-up logic resets the 6707 microprocessor, Stepper Motor logic, Peripheral Interface Adaptor (PIA) and Data Interface section (2793 FDC and Analog circuitry) whenever the drive is turned on. In addition, the power-up logic circuit locks the Data Output Buffer off during the short period when the drive is tuned on. This prevents random pulses generated by the drive's circuitry (during the initialization period) from being sent to the console.

The RESET logic returns the electrical circuits to their starting conditions.

ELECTRONIC THEORY

The 1050 Disk Drive consists of eight major electronic elements. These include:

- Power-up logic (discussed in the Power Supply section above)
- Clock
- 6507 Microprocessor Unit (MPU)
- Read-only Memory (ROM)
- Random Access Memory (RAM)
- 6532 Peripheral Interface Adaptor (PIA)
- 2793 Floppy Disk Controller
- Read/Write and Erase Logic

Functional block diagram of the electronic elements of the 1050 Disk Drive follows (Figure 1-6), along with a discussion of each.

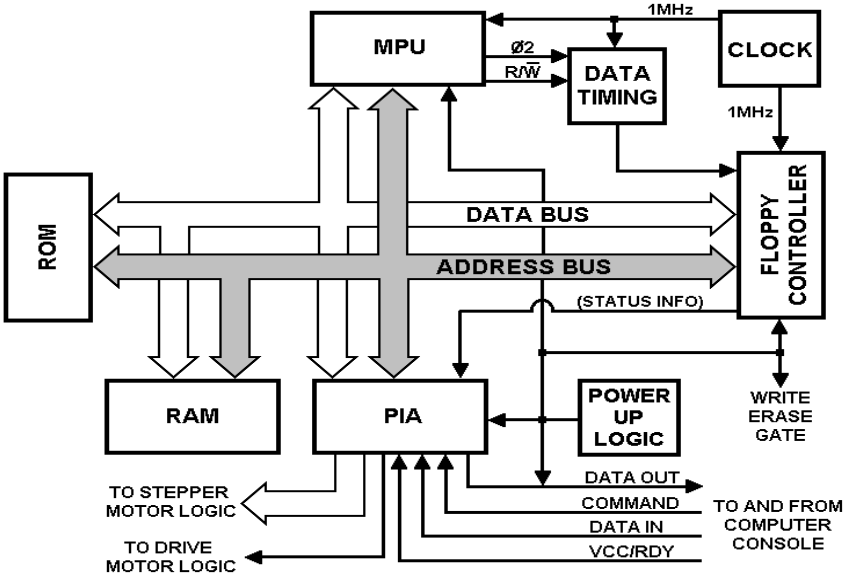


Figure 6. Disk Drive Electronic Units

6507 MICROPROCESSOR

The Disk Drive's 6507 microprocessor (MPU) provides the primary decision making and computational capabilities for the drive. It is a self-contained microcomputer system on a single chip.

The MPU controls the sequence of system operations by putting addresses out to the program memory (ROM) and receiving instructions in return. It causes the system to perform the desired operation by reading an instruction (specific bit pattern) and executing that instruction. It then goes to the next instruction in the program and executes it.

The microprocessor:

- Controls the 2793 or 2797 Floppy Disk Controller (FDC)
- Monitors the Peripheral Interface Adaptor (PIA) for data transfers and status requests by the computer console.
- Controls the Stepper Motor Logic, Disk Drive Logic and Motor Logic, all of which are buffered in the P IA.
- Provides control characters to notify the computer console of the status of operations performed and information received.
- Executes commands from the computer console.
- Controls data transfers through control of the common data and address buses.

The address bus, the bi-directional data bus, and the Read/Write line serve as parallel paths for data transfer in end out of the microprocessor and give it direct control over the central processing system. The address bus puts out addresses to control the source or destination of data transfers. The Read/Write line determines the direction in which data transfer occurs.

These addresses are derived from various sources within the microprocessor. During the instruction cycle from program memory (ROM), the addresses are usually derived from the program counter which controls the execution of sequential instructions. Addresses for data transfers between the microprocessor and RAM are usually derived either directly from the program memory or from the microprocessor.

6532 PERIPHERAL INTERFACE ADAPTOR (PIA)

The 6532 Peripheral Interface Adaptor (PIA) is a buffering and signal: formatting device with no decision making or computational capability. It is an Input/Output (I/0) device which acts as an interface between the 6507 microprocessor, the 1050 system functions and the console.

The PIA

- Monitors the 2793 or 2797 Floppy Disk Controller.
- Provides 128 bytes of RAM for temporary store of status information and data sent by the Data Interface section for application to the microprocessor.
- Applies the console's serial outputs to the data and address buses when requestd to do so by the drive's microprocessor unit.
- Acts as communication interface between the computer console and the microprocessor.
- Interfaces with the Stepper motor Logic and Drive Motor Logic.

The microprocessor communicates with the PIA through eight data lines connected to the data bus. The microprocessor initiates communication by using its address lines to select or address the P IA.

The PIA provides 16 programmable bi-directional port lines to communicate with the computer console and perform the system functions. The port lines are divided into two 8-bit ports, PAO-PA7 and PBO-PB7. PA7 may also function as an interrupt input pin.
The Interrupt Request (IRO) line is used to inform the microprocessor when a device requires servicing.

2793 OR 2797 FLOPPY DISK CONTROLLER

The 1050 disk drive will contain either a 2793 or 2797 Floppy Disk Controller IC depending on the date of manufacture of the drive.

The 2793 or 2797 Floppy Disk Controller (FDC) and the Read/Write and Erase Logic make up the Data Interface between the disk drive's central processing system and the diskette. Pin 25 of 2797 should be out of socket.

The FDC is the main element of the Data Interface function. The FDC is a highly specialized microprocessor which has an arithmetic logic unit, comparator and the necessary microprogram logic to control the Read/Write operation to the diskette. It also includes an internal phase-lock loop, data separation and write precompensation logic.

The FDC:

- Combines data, timing and data validity pulses into the serial format for recording onto diskette.
- Separates the above signals and provides the output data in parallel during a Read operation.
- Controls the Write and Erase logic circuitry during a Write operation.
- Generates the data validity codes (called Cyclic Redundancy Checks or CRCs) during a Write operation and checks them during a Read operation.
- Contains an internal phase-lock loop.

The microprocessor controls the FDC and can access any of the following registers located in the FDC: Track, Sector, Data, Command, and Status. The following is an explanation of the contents of each register.

Track Current head address. Updated automatically as the head moves across the diskette.

Sector Number of the sector being considered for a Read or Write operation.

Data Information read from the diskette to be transferred to the microprocessor after the necessary serial-to-parallel conversion. The FDC receives data in parallel from the microprocessor and converts the data to serial for storage on the diskette.

Command Instructions from the microprocessor that are interpreted by an internally controlled programmable logic array to generate the appropriate control signals for the logical operation to be performed.

Status Condition of the system. After each command is executed, the control logic issues an interrupt to the microprocessor to allow examination of the status register for any errors before resetting the interrupt. Each of the eight bits in the status register represents a different error condition.

The FDC controls the following elements of the Data Interface function:

- Read/Write Head
- Erase Head
- Read Logic
- Write/Erase Logic
- Write Protect Logic

CLOCK

The clock generator produces a continuous waveform that controls all signal transitions in the system. It provides timing controls for the 1050 Disk Drive Logic and the Read/Write operations to the diskette.

The drive's clock circuitry generates a crystal controlled 1 MHz signal. The 1 MHz signal is used by the 2793 or 2797 Floppy Disk Controller (FDC) and Write/Erase gate for timing serial data to the heads. It is also used by the 6507 microprocessor to clock parallel data into and out of the FDC.

READ-ONLY MEMORY (ROM)

The Disk Drive's Read-Only Memory (ROM) stores the sequence of instructions (program memory) that make up the 1050's internal control software. It contains specific operating instructions used by the microprocessor to accomplish a variety of functions. These functions include telling the 2793 or 2797 Floppy Disk Controller (FDC) what task to perform.
An important characteristic of the ROM chip is that the information is stored on a permanent basis. Turning OFF the power does not cause the loss of ROM information.

RANDOM ACCESS MEMORY (RAM)

The Disk Drive's Random Access Memory (RAM) is used by the microprocessor for temporary storage of Input data, calculations and system information.

Data may be written into RAM as well as read from RAM by the microprocessor. The RAM Identifies the type of data transfer by the Read/Write line. When the line is active HIGH, the operation is to Read from memory and when the line is active LOW, the operation is to Write to memory. Turning the power OFF obliterates all information in RAM.

WRITE/ERASE LOGIC

The Write/Erase Logic manages the recording of data from the Floppy Disk Controller to the diskette. It provides correct current and polarity to the Read/Write Head.

The Write Driver enables Write functions and limits the Write currents.

The Write and Erase Gate turns on both the Write and Erase Drivers during a Write operation and turns them off during a Read operation.

The Erase Driver drives the Erase Head during a Write operation.

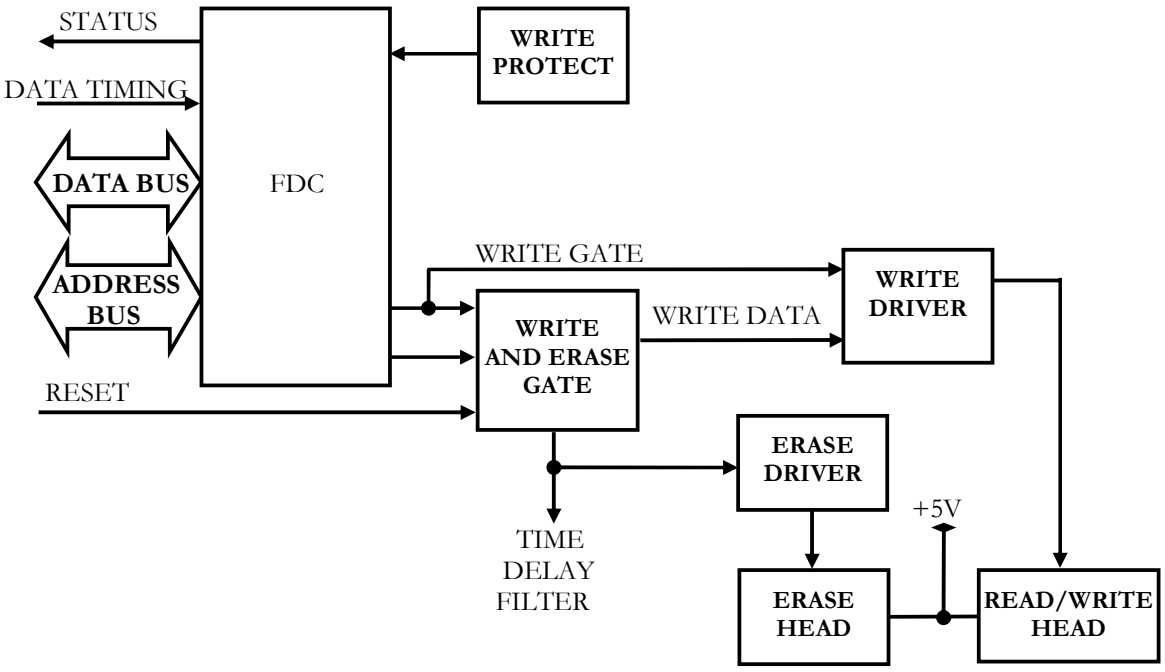


Figure 7. Write/Erase Logic Block Diagram

WRITE-PROTECT LOGIC

The Write-Protect Logic prevents writing to a diskette by informing the Floppy Disk Controller when a write-protected diskette is inserted in the drive. Each diskette contains a notched area in the upper right hand corner which allows light from the LED to hit the base of the phototransistor. On a write-protected diskette the light is blocked by a tab or opaque material on the diskette. This turns off the phototransistor and the output from U11 is clamped Low. The low input to the FDC signals that a write-protected diskette is inserted and you cannot write to it.

READ LOGIC

The Read Logic is used to retrieve data from the diskette and input the data into the FDC. It shapes pulses into the correct format to be read by the FDC.

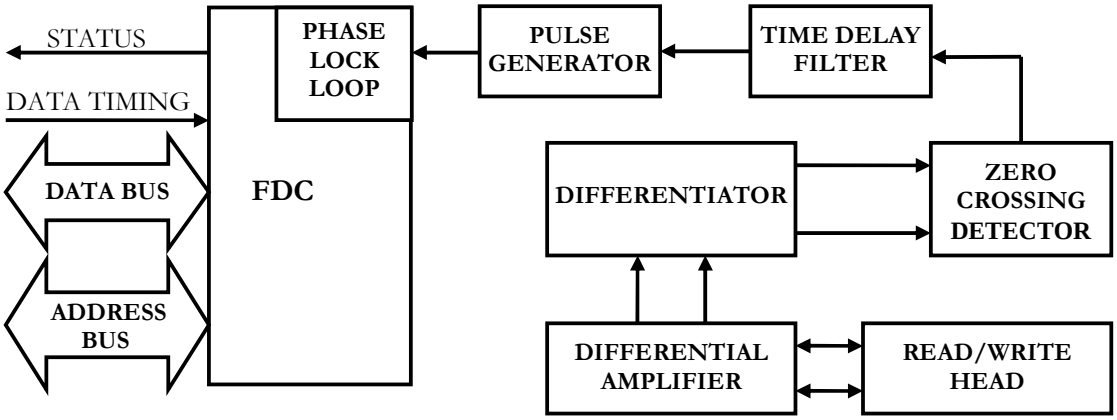


Figure 8. Read Logic Block Diagram

The DIFFERENTIAL AMPLIFIER provides initial amplification of READ/WRITE HEAD signals.

The DIFFERENTIATOR squares up the two DIFFERENTIAL AMPLIFIER outputs.

The single output Zero Crossing Detector changes level whenever the two 180 degree out-of-phase input signals cross their zero axis coincidentally. This eliminates false pulses caused by READ/WRITE HEAD signal decay, rather than intentional signal level changes.

The TIME DELAY FILTER is a digital filter.

The PULSE GENERATOR produces a single pulse out for each logic level transition at its output. This results in the reproduction of the original FDC signal.

READ/WRITE HEAD

The READ/WRITE HEAD is an electro-magnetic device used for interfacing with the magnetic recording media. It converts magnetic flux changes to electric current, and vice versa, through the use of a center tapped coil.
Current is passed through the windings on the head core. Data is written to the diskette surface by changing the direction of the current through the READ/WRITE HEAD (each flux change equals a data bit).

Data is read from the diskette when signals from the head coil windings are applied to the differential amplifier.

ERASE HEAD

The ERASE HEAD creates a guardband (a blank space between tracks) in order to prevent one recorded track from interfering with either the next inner or next outer track.
It straddles the Read/Write Head in such a way that after the data is written onto the diskette, the Erase Head "tunnel" narrows the track width, leaving guardbands between tracks.

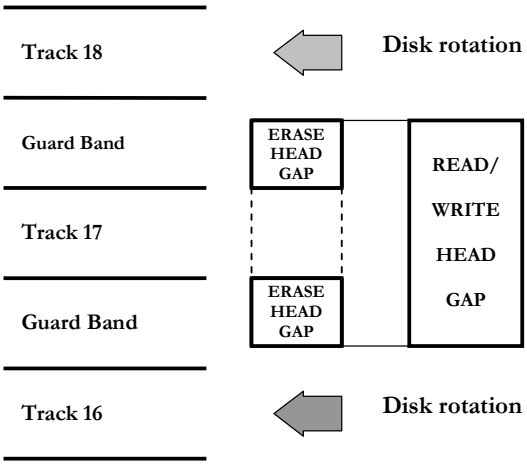


Figure 9. Erase Head Gaps

SERIAL BUS LINE ASSIGNMENTS

The computer communicates with peripheral devices via a serial port which consists of a serial DATA OUT (transmission) line, a serial DATA IN (receiver) line and miscellaneous control lines.

Data is transmitted and received as 8 bits of serial date (least significant bit sent first) preceded by a logic zero start bit and succeeded by a logic one stop bit. The serial DATA OUT is transmitted as a positive logic (+4V = one/true/HIGH, 0V = zero/false/LOW). The serial DATA OUT line always assumes its new state when the serial CLOCK OUT line goes HIGH; CLOCK OUT then goes LOW in the center of the DATA OUT bit time.

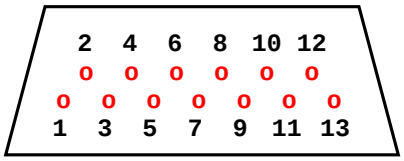


Figure 10. PERIPHERAL Connector

1 CLOCK IN is not used by the current DOS and peripherals. This line is reserved for future synchronous communications.
2 CLOCK OUT is the serial bus clock. CLOCK OUT goes HIGH at the start of each DATA OUT bit and returns to LOW in the middle of each bit.
3 DATA IN is the serial bus data line to the computer.
4 GND is the signal/shield ground line.
5 DATA OUT is the serial bus data line from the computer.
6 GND is the signal/shield ground line.
7 COMMAND is normally HIGH and goes LOW when a command frame is being sent from the computer.
8 MOTOR CONTROL is the cassette motor control line (HIGH = on, LOW = off).
9 PROCEED is not used by the current DOS and peripherals. This line is pulled HIGH passively inside the computer.
10 +5V/READY indicates that the computer is turned on and ready. This line may also be used as a +5 volt supply of 50liA current rating, for Atari peripherals only.
11 AUDIO IN accepts an audio signal from the diskette.
12 +12V supply for Atari peripherals only (not used in 1050).
13 INTERRUPT is not used by the current DOS or peripherals. This line is pulled HIGH passively inside the computer.

SERIAL BUS ELECTRICAL SPECIFICATIONS

Peripheral Input:

VIH = 2.0 V minimum
VIL = 0.4 V maximum

I IH = 20 μA maximum at VIH = 2.0V
IIL = 5 μA maximum at VIL = 0.4V

Peripheral Output (open collector bipolar):

VOH = 4.5 V minimum with external 100 kΩ pull-up
VOL = 0.4 V maximum at 1.6 μA

Vcc/READY Input:

VIH = 2.0V minimum at IIH = 1 μA maximum
VIL = 0.4V maximum
Input goes to logic zero when open

SERIAL BUS PROTOCOL

When a command line goes LOW, the computer console sends a command frame to all devices. The command provides the disk drive with the following information:

- Serial Bus Device ID
- Command
- Two bytes of auxiliary information
- Checksum

The commands suppported by the disk controller are: Get Sector, Put Sector, Put Sector with Verify, Status Request, and Format Disk.

SECTION 2

1050 SPECIFICATIONS

Functional Specification

Key Features

- Lower Cost than 810.
- Fully compatible with 810 in single density (FM) mode.
- Double Density read/write operation using MFM encoding.
- Fully compatible with existing Atari disk operating system.
- Fully support the Atari SIO interface and protocol.
- Support new high level macro command requested by next generation Atari disk operating system.

Disk Drive Specification

	Single Density (Read/Write)	Double Density (Read/Write)
Tracks per surface	40	40
Tracks per inch	48	48
Recording Density (track 39)	2,878 BPI	5,757 BPI
Flux Density (track 39)	5,757 FCI	5,757 FCI
Encoding Method	FM	MFM
Capacity unformatted:		
Per Track	3,382 Bytes	6,510 Bytes
Per Surface	135,280 Bytes	260,400 Bytes
Capacity formatted:		
Sectors/Track	18	26
Bytes/Sector	128	128
Bytes/Track	2,304	3,328
Bytes/Surface	92,160	133,120
Transfer rate	125,000 BPS	250,000 BPS
Read/Write Head	1	1
Write Protect Sensor	Yes	Yes
Track 00 Sensor	Yes	Yes
Rotational Speed	288 RPM	288 RPM
Rotational Speed Accuracy	± 3%	± 3%
Average Latency	110 ms	110 ms

	Single Density (Read/Write)	Double Density (Read/Write)
Access Time (max):		
Track to Track	40 ms	40 ms
Head Setting	30 ms	40 ms
Motor Start	1000 ms	1000 ms

Media Requirements:

Single Density: Soft Sectored, per Atari specification (#CO16884)
Double Density: Soft Sectored, per Atari specification (#CO16890)

Physical and Dimensional Specification:

Drive outside dimension (exclusive of front panel)

HEIGHT	1.70 inches max.
WIDTH	6.00 inches max.
LENGTH	8.00 inches max.
WEIGHT	6 Pounds max.

Electrical Specification:

Drive Read/Write Electronics

Head Voltage at 1F amplitude	10 mV max. at Track 00
Head Voltage at 2F amplitude	3 mV max. at Track 39

These data values should be obtainable from various diskette vendors.

Power Specification:

AC Power Adaptor (North America Version):
Consult the Atari 31 VA AC Power Adaptor Specification (# CO17945)

AC Power Adaptor (International Version) TBD

System Electronics
Including Drive Electronics, Controller Electronics and Power Supply Electronics:

Input Voltage	8.52V AC ±12% @ 60Hz ±3Hz

Power Consumption:

Standby	15 W max.
Operating	30 W max.
Start Up	50W max.

SECTION 3

DISASSEMBLY/ASSSEMBLY

Turn the unit over and remove the four screws from the bottom cover and the two screws holding the lower part of the front bezel (see figure).
Holding the top and bottom covers together, turn the unit right side up.
Carefully pull the lower part of the front bezel forward and at the same time lift off the top cover. (Be careful not to break the thin plastic tabs attaching the top of the front bezel to the top cover).
The drive mechanism rests on four dowels above the Printed Circuit Board. To remove it, disconnect the plugs from the PCB and lift it out. When reattaching, be sure to note the correct polarity of the plugs (see figure).
The PC board snaps into the bottom of the lower cover and fits over the three alignment guides located in it.
The upper and lower RF shields are attached to the PCB by four bend tabs. When removing the top shield, be sure to note where the cutouts are located and replace it the sane way.
The five LSI's are located under the shield No adjustment to the variable capacitor or resistors is needed when replacing the 2793 or 2797 Floppy Disk Controller chips.
Reassemble in the reverse order.

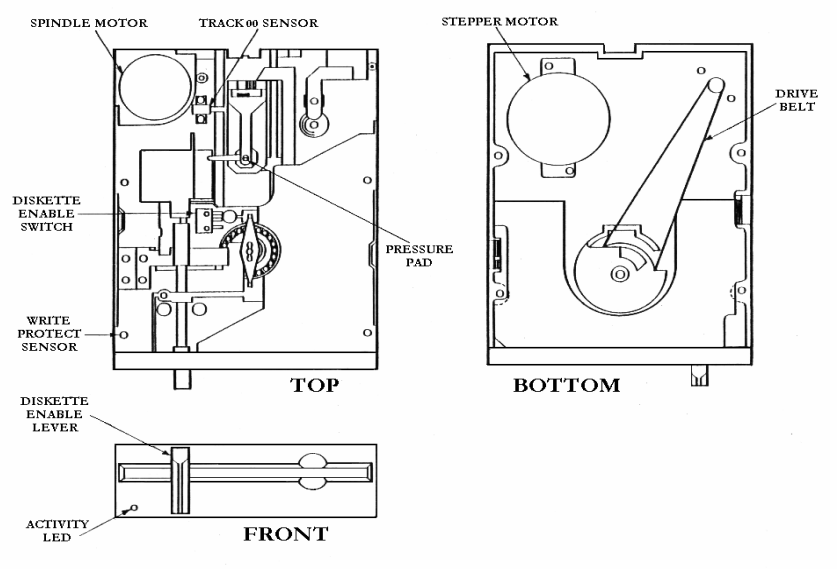


Figure 11. 1050 Drive Mechanism (Tandon)

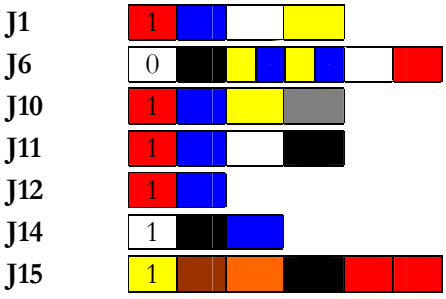


Figure 12. Plug Connections of 1050 Mechanism

SECTION 4

DIAGNOSTIC TESTINGS

Equipment Requirements:

- 400 Computer with 16K of RAM
- Television
- Oscilloscope at least 15MNz Digital Voltmeter
- ATARI 1050 Disk Drive Diagnostic Diskette (FD 100690)
- Dymek Alignment Diskette (TEO 17575)
- Work Diskette (FD 100053)
- Preformatted Diskette(FD 100026)
- Assorted Small Tools
- Printer (Optional)

Hook Up

- Set up the disk drive and computer according to the procedures in the 1050 Owner's Guide.
- Set the drive select switches to the Drive 1 position.
- Be certain all connections ere secure.

Check Of Mechanical Components:

- Before testing the Disk Drive, be certain of the following:
- Check that the diskette enable lever moves freely and locks in the perpendicular position.
- Insert a diskette in the slot and push it all the way in. Make sure that the eject mechanism clicks into position. Now move the diskette enable lever around to the perpendicular position to lock. Make sure that the diskette is ejected when the diskette enable lever is returned to the parallel position.

Diagnostic Tests

The tests in this section are intended to assist you in diagnosing possible problems in the 1050 Disk Drive. All diagnostic and functional tests are reviewed in this section. Use these tests in conjunction with the troubleshooting guide, waveform diagrams, and schematics to troubleshoot the unit under test.

Power Up Test

Purpose: To test the disk drive's electronic hardware Initialization and Reset. This test prepares the drive for further testing. The drive must pass this test before any other tests can be performed.

Special Tools Required: None

Procedure:

1. Connect disk drive to computer.
2. Turn the disk drive power switch ON.
3. Observe that the following occur:
   a. The Power LED lights.
   b. The Activity LED lights.
   c. The Drive Motor turns on.

d. The Head Carriage steps to track 00 (outer track).
e. Several seconds pass, and the Drive Motor and the Activity LED turn off.

4. This completes the Power-up Test.

This test indicates that the unit passed all of its internal diagnostics. The internal diagnostic test checks the following six elements:

1. Input/Output Device
   The 6532 device is initialized and verified. Upon incorrect comparison, the processor will flag ERROR.
2. Disk Controller Device
   The 2793 or 2797 device is tested for ass to the track, and sector registers, followed by an internal functional test. Upon error, the processor will flag ERROR.
3. ROM Checksum
   The processor verifies PROM validity by performing a checksum on it. Upon error, the processor will flag ERROR and discontinue testing.
4. RAM Check
   Unique values are written to each RAM location, and then each location is read to verify It contains the correct value. Upon error, the processor will flag ERROR and discontinue testing.
5. Error Flag Stop
   Upon any ERROR flag being set, the processor will discontinue testing and place the unit in a hard failure state (2-second cycle off/on of spindle motor).
6. Restore Check
   Track 0 is sought by stepping the head away from spindle until track 0 sensor is detected and motor phase is 1. Upon stepping more than 50 tracks without finding the track 0 sensor, the unit will fail and enter the hard failure state.

Loading The Diagnostic Test Diskette

Insert the Diagnostic Diskette and turn the diskette enable lever down. The activity LED lights, and the motor spins for about five seconds, centering the diskette on the spindle.
Now Power-Up the computer without a cartridge installed The Diagnostic Test will boot-up and display the two main menu options on the TV screen.

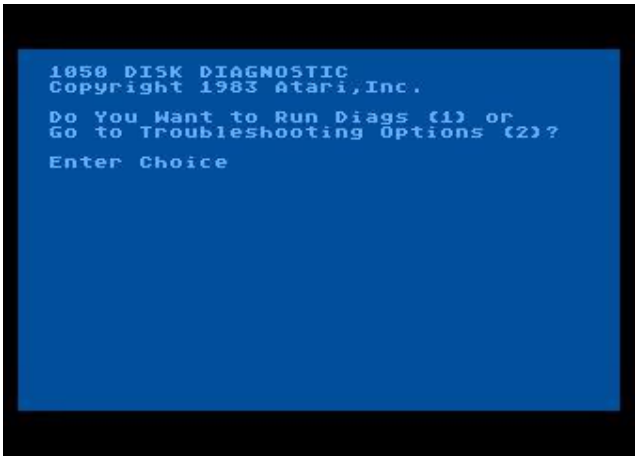


Figure 13. 1050 Disk Diagnostic Screen

Make selection 1 and hit the RETURN key. The diagnostic testing will run automatically.

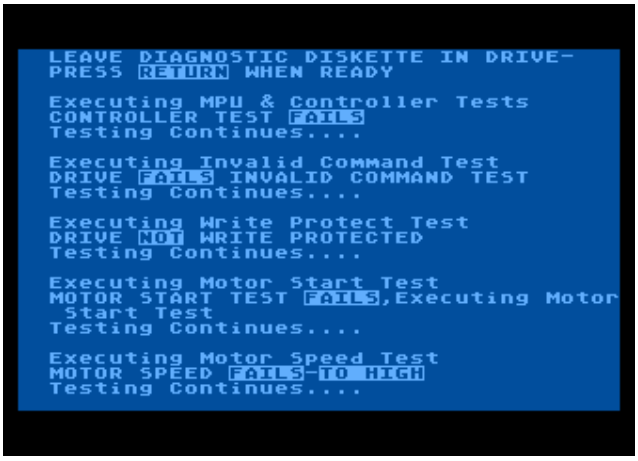


Figure 14. Running 1 Option…

These pass or fall tests will indicate which section of the disk drive to start your troubleshooting in. The following is a detailed description of each test.

MPU & Controller Test

This checks that the 2793 or 2797 floppy disk controller chip will recognize a command or data frame from the computer. A failure here indicates a defective 2793 or 2797 IC.

Invalid Command Test

This checks that the 2793 or 2797 floppy disk controller chip .will recognize an illegal command or data frame and not try to execute on it.

Write Protect Test

This checks out the Write Protect Sensor and related circuitry.
* If Write Protect is constantly on, check to be sure that dirt has not blocked the hole where the lower part of the sensor is located.

Motor Start Test

This test checks the elapsed time between starting the spindle motor from a dead start to the point where valid data is read from the diskette. If this test fails a motor control circuit or a read circuit failure is indicated.

Motor Speed Test

This test checks the speed of the spindle motor in milliseconds. If the speed is too low or too high use the speed calibration option in the troubleshooting section of the Diagnostic Program Disk to adjust (VR2) with a screwdriver.

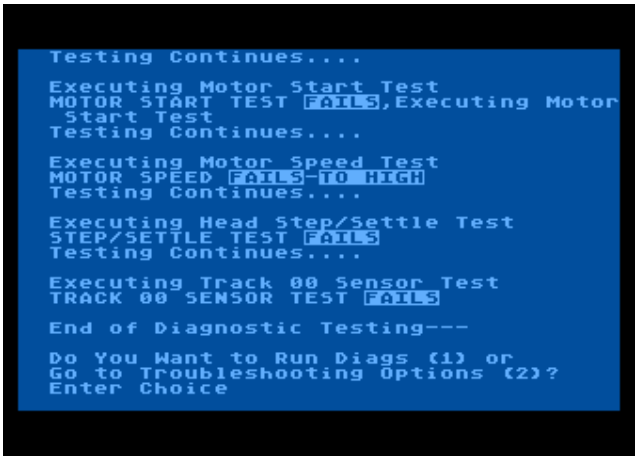


Figure 15. Running 1 Option (continued)

Head Step & Settle Test

This test checks the capability of the drive to read a sector, step to the next track, ark read another sector within a specified amount of time. A failure here would indicate a bad drive mechanism, or a defect in the read circuitry.

Track 00 Test

This test steps the Read/Write Head out to track 02 then steps back to track 00 and checks the status of the track 00 sensor. If this test fails, use the track zero sensor calibration option in the troubleshooting section of this diagnostic program to adjust the sensor.

At the end of the Diagnostic tests, you are again given the choice of:

(1) Run Diagnostic Tests
(2) Troubleshooting Options

Select 2 and hit RETURN. This will give you the troubleshooting options menu.
This section combined with the troubleshooting guide, circuit waveforms, and schematics, will help you to troubleshoot or make adjustment to various circuits in the 1050 disk drive.
Read the instructions and follow the prompts, displayed on the screen, carefully.
The following is a detailed description of the troubleshooting options:

Figure 16. Troubleshooting Options List

Loop on Speed Calibration

Use this option to set the spindle speed.

Figure 17. Motor Speed Test

Adjust VR2 for a speed of 208.3 milliseconds ±1.0 msec.

Run Manual Alignment Tests

The following four tests are designed to check out the drive mechanism alignment. Use the Dymek Analog Alignment Diskette (Part # TE017575).

Set the oscilloscope as follows:

Channel A	Normal
Channel B	Inverted
Vertical Mode	Add. Ch. A&B
Time/Div	2ms/Div
Volts/Div	20mV/DIv (X10 Probes)
	AC (Ch. A&B)
Trigger	Internal (Ch A), AC, Normal,
	Positive slope

Set up the probes as follows:

Channel A	TP 3 on PCB A
Channel B	TP 4 on PCB A
Ground TP	17 on PCB A

Use track 0 to double check the spindle speed of the drive mechanism on track 00. The time for one cycle of the sinewave is approximately 16.6ms.

Use track 16 to check or adjust the radial track alignment.

(Cats-Eyes). Set the time/div at 20ms/Div and follow the instructions below.

Verify that cats-eyes lobes are present on the oscilloscope and observe the lobe ratio of the cats-eyes. The lobe ratio is the amplitude of the smaller lobe divided by the amplitude of the larger lobe. The ideal lobe ratio is 100% (both lobes equal). See figure below.

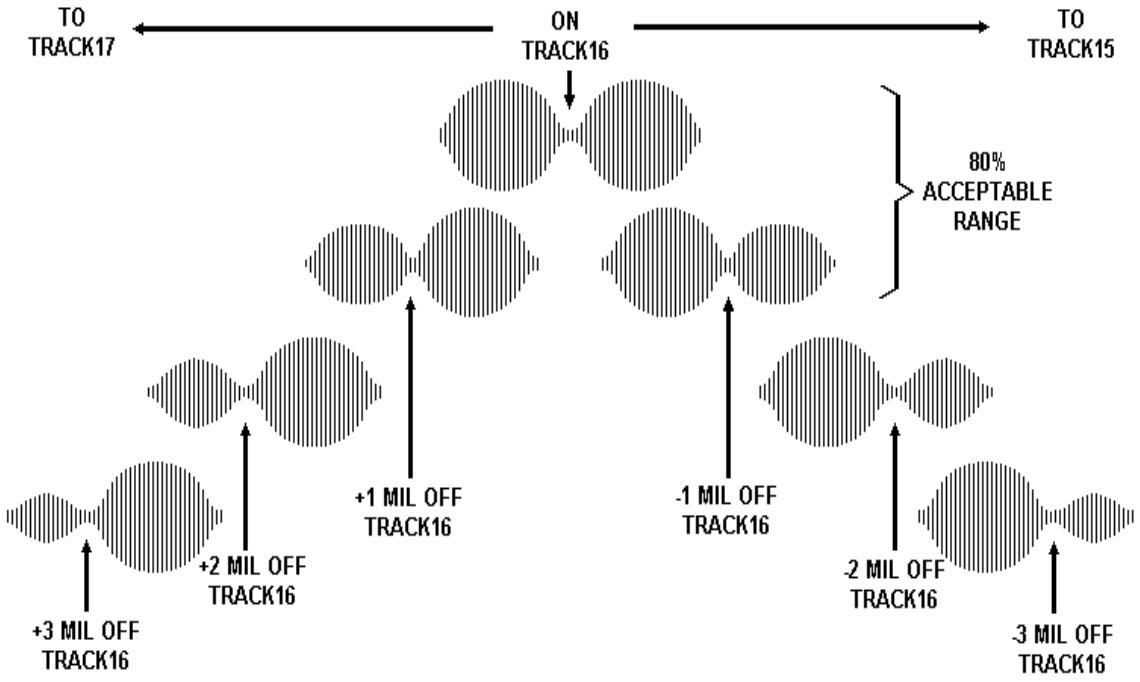


Figure 18. Cat-Eyes waveforms

Align the TM50-1 drive by loosening the screws on the stepper motor and then rotate the motor until the lobe ratio is 100%. Recheck the track 0 sensor adjustment, then recheck lobe ratio. Repeat until the alignment is within 80%-100%. Tighten down stepper motor screws.

Use track 33 to check the Head Load Pad Pressure. Set the time/div to 0.5 ms/div, and set the volts/div to 50 mV/div.

There should be a broadband display on the oscilloscope. With your index finger press very lightly on the top of the pressure pad. If the amplitude increases greatly (more than 20%) then use a flat blade screwdriver to turn the pressure pad 1/4 of a turn at a time. After 3/4 of a turn assume the pressure pad to be bad and replace it.

Use track 34 to check the Head Azimuth. Set the time/div for 0.5ms/div, and set the volts/div for 50mV/div.

See the following diagrams for the correct waveforms.

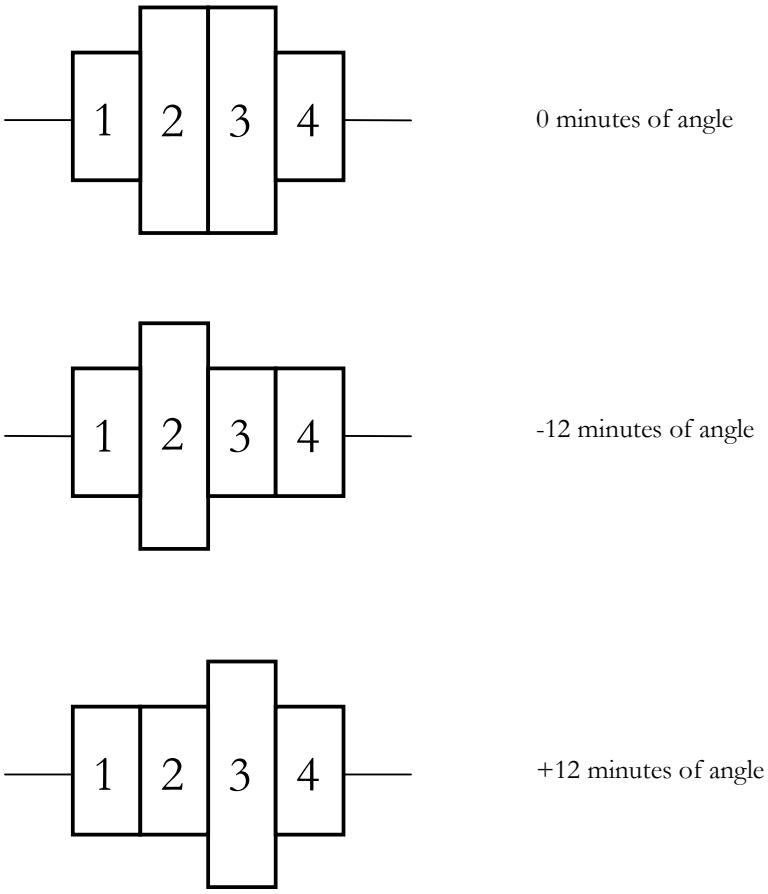


Figure 19. Head Azimuth waveforms

If the Azimuth is greater than ±18 minutes of angle, replacement of the entire drive mechanism is recommended due to the complexity of the adjustment.

Use the ESC key to stop the test, and the RETURN key to return to the menu.

Drive Select Switch Test

This test is to assure that the disk drive can be selected in all four positions. Check all four positions, then return to drive #1 position. There is a slight delay and then an automatic return to menu when this test is done.
If this test fails in any position, check out the switch first, and PIA chip second.

Single Density Burn-in (10 min)

This is a short test to check for compatibility between drives. A failure on this test indicates an alignment problem. (See Option 2 on troubleshooting options.)
This test first does a write to alt sectors (E5 pattern), then it does a read of all sectors. Be sure to use preformatted diskette #FD100026.

Double Density Burn-In (2 hours)

This test formats the diskette in double density, writes and reads all data fields with a sequential seek, and writes and reads all data fields with an according seek.
Errors are logged into the first and third sector on the track where they occur. These errors can be printed out on the printer using the printout option in the troubleshooting options of the diagnostic test program. If the 1050 should be disconnected from the SIO line once this test has been started the testing will continue until the pass counter reaches zero. This test will abort if:

1. The drive fails to format or verify format.
2. The drive fails to read or write the error logs (sectors 1 or 3 on each track).
3. More than 128 errs occur in any one sector.
6. Error Printout

This option is used in conjunction with the double density burn-in described above to printout the error logs written on each track.
The following are two examples of this printout and how to interpret them.

```
1050 BURN-IN (2HR), REV. A
SERIAL I.D. - 3456789012

PASS COUNTER = 0
PASS COUNT RECEIVED = 24

TRACK 31 -ERRORS
  SECTOR 16 ERROR STATUS - $01
  DATA BYTE LOCATION = 47

  DATA DATA DATA DATA SEEK RNF
  CRC  LOST HARD SOFT
  0    0    0    1    0    0

TRACK 31 -ERRORS
  SECTOR 20 ERROR STATUS -$02

  DATA DATA DATA DATA SEEK RNF
  CRC  LOST HARD SOFT
  1    0    0    0    0    0

TRACK 33 - ERRORS
  SECTOR 4 ERROR STATUS = $01
  DATA BYTE LOCATION - 77

  DATA DATA DATA DATA SEEK RNF
  CRC  LOST HARD SOFT
  0    0    0    1    0    0
```

Figure 20. Example 1 of Error Printout

```
1050 BURN-IN (2HR), REV. A

SERIAL ID. - 1234567890
PASS COUNTER = 24
PASS COUNT RECEIVED = 24

NO ERRORS - ALL TRACKS
```

Figure 21. Example 2 of Error Printout

Example 1 is an example of the error logs which are recorded during the double density burn-in routine. Example 2 is an example of the printout from a perfect burn-in test.

The use of this error printout is quite subjective. You may have several errors and still have a good drive. We will attempt to give you a feel for what the major concerns are.

The first thing to look at is the pass counter. This should equal the number in the pass count received, which indicates that the drive performed burn-in with no major failures.
The next thing to look for is many errors of the same type located on the same track and/or sector. If this situation occurs, run the burn-in test again using a different blank diskette. If the problem still exists, there is probably a hardware failure.

The next thing to look for is the type of error most commonly found. Below are some clues as to the cause of the error types:

Data CRC - If several of these errors occur, replace the 2793 or 2797 controller IC. Troubleshoot the read and write circuits.

Data Lost - This indicates a problem in transferring data between the 2793 or 2797 and the 6810 RAM IC.

Data Hard - This occurs when data cannot be found after many retries. Check the write circuit and the diskette for flaws.

Data Soft - This indicates that data was not read on the first pass, but in subsequent passes was found. If many of these occur in different locations suspect the speed adjustment or 2793/2797.

Seek - Many seek errors would indicate a bad diskette or an alignment problem (cats-eyes).

RNF - Many RNF errors in the same location would indicate a bad diskette. Many RNF errors in different locations indicates a bad WD2793/2797 controller.

Track 00 Sensor Calibration

This option is used to check and adjust the track zero sensor.
If the sensor is misadjusted, the screen will display either "forward" or "backward" indicating which direction the sensor needs to be moved. To adjust the sensor, loosen the screw holding it in place and move the sensor backward or forward as dictated by the screen until the screen displays "sensor OK".

Figure 22. Track 0 Sensor Calibration Test

Be careful ! This is a slight adjustment which does not take much movement to correct. Hold the sensor in position while tightening down the screw.

SECTION 5

SYMPTOM CHECKLIST

DRIVE MOTOR AND SPEED PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Drive motor doesn't rotate when latch is shut (no Activity LED)	Defective Diskette Enable switch	Replace Diskette Enable switch assembly on drive mechanism.
	Intermittent or bad connection	Check that P1 is properly connected to J1
	Defective diskette enable circuit (U6)	Troubleshoot and replace defective component (see waveforms, p. 4-8)
	Defective component in motor control circuit (Q4, Q6, U5, VR2)	Troubleshoot and replace defective component (see waveforms, p. 4-9)
	Defective drive motor	Replace drive motor
Drive motor operates sporadically	Intermittent or bad connection	Check that P1 is properly connected to J1
	Defective component in motor control circuit (U5, VR2, Q4, Q6)	Troubleshoot and replace defective component (see waveforms, p. 4-8)
	Defective component in tachometer feedback circuit (U5, VR2, Q6)	Troubleshoot and replace defective component (see waveforms, p. 4-9)
	Open winding in drive motor tachometer.	Replace drive motor
Drive motor speed too slow or too fast	Speed adjustment incorrect	Adjust speed POT (VR2) for speed of 208.3 ms
Speed not adjustable	Defective component in tachometer feedback circuit (U5, VR2, Q6)	Troubleshoot and replace defective component (see waveforms, p. 4-9)
	Open winding in drive motor tachometer.	Replace drive motor
Drive motor speed unstable	Intermittent or bad connection	Check that P1 is properly connected to J1 (refer to figure 3-1)
	Drive belt slipping	Replace drive mechanism
	Defective component in tachometer feedback circuit (U5, VR2, Q6)	Troubleshoot and replace defective component (see waveforms, p. 4-10)
	Drive motor bearings	Replace drive motor

STEPPER MOTOR PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Head positioner will not step	Bad connection at J15	Check for proper connection and polarity at J15 (refer to figure 3-1)
	Defective component in stepper driver circuit (U2, U3, U7)	Troubleshoot and replace defective component (see waveforms, p. 4-10)
	Defective stepper motor	Replace drive mechanism
Skips or missteps to wrong tracks	Bad connection at J15	Check for proper connection and polarity at J15 (refer to figure 3-1)
	Defective component in stepper driver circuit (U2, U3, U7)	Troubleshoot and replace defective component (see waveforms, p. 4-10)
	Band pully or head carriage binding	Replace drive mechanism
	Track 00 sensor defective need adjustment Q5	Troubleshoot and replace or adjust defective component (see waveforms, p. 4-10)

DRIVE MECHANISM PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Diskette will not eject	Eject assembly binding or broken	Replace drive mechanism
Drive will not pass track 00 sensor test	Track 00 sensor defective or needs adjustment	Troubleshoot and replace or adjust defective component
	Carriage stop missing or improperly set	Replace drive mechanism
	Defective component in track 00 sensor circuit	Troubleshoot and replace defective component (see waveforms, p. 4-11)
Intermittent Read/Write errors	Head load pad pressure	Replace drive mechanism
	Dirty Read/Write head	Clean head with 91% Isopropyl Alcohol
	Burned head	Replace drive mechanism
Diskette incompatibility	Radial track alignment	Adjust "Cat's Eyes" alignment
	Head azimuth alignment	Check head azimuth. If out of spec., replace drive mechanism
	Drive belt slipping	Replace drive mechanism
	Speed improperly adjusted (VR2)	Check and adjust for proper speed on both drives

READ PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Soft Read errors (intermittent or non-permanent)	Defective Diskette	Try diskette on known-good drive
	Dirty Read/Write head	Clean head with 91% Isopropyl Alcohol
	Drive belt slipping	Replace drive mechanism
	Excessive noise in Read signal (U13, U18-20, U22-24)	Troubleshoot Read circuit (see waveforms, p.4-12)
	Intermittent or marginal component I Read circuit (U13, U18-20, U22-24)	Troubleshoot Read circuit (see waveforms, p.4-12)
Fails to read anything	Improper connection of J6	Check for correct polarity (refer to Figure 3-1)
	Failed component in read circuit (U13, U18-20, U22-24)	Troubleshoot and replace failed component (see waveforms, p. 4-12)
	Burned head	Replace drive mechanism
	Speed adjustment incorrect	Adjust speed POT (VR2) for speed of 208.3 ms
	Head load pad pressure	Replace drive mechanism
	Dirty Read/Write head	Clean head with 91% Isopropyl Alcohol
	Radial track alignment	Adjust "Cat's Eyes" alignment
	Head azimuth alignment	Check head azimuth. If out of spec., replace drive mechanism

POWER SUPPLY PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
No power or blows power	Defective bridge diodes	Replace all four diodes (CR17-CR20) (see waveforms, p. 4-16)
	Defective power adaptor	Replace power adaptor
No +5V at TP13	Defective 5V regulator	Replace Q7
Power LED not lit	Defective 5V regulator	Replace Q7
	Defective LED	Replace CR21
No +12V at TP14	Defective 12V regulator	Replace Q8
	Defective12V doubler circuit	Replace CR15 and CR16, or C71 (see waveforms, p.4-16)

WRITE PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Fails to Write anything	Improper connection of J6	Check for correct polarity (refer to Figure 3-1)
	Dirty Read/Write head	Clean head with 91% Isopropyl Alcohol
	Defective Write protect circuit (U11, U13)	Troubleshoot and replace defective component (see waveforms, p. 4-13)
	Component failure in Write circuit (U13, U15-18, U21, Q1)	Troubleshoot and replace defective component (see waveforms, p. 4-14)
	Defective component in Erase circuit (U11, U15, U17)	Troubleshoot and replace defective component (see waveforms, p. 4-15)
	Burned head	Replace drive mechanism
Error 144 during Write or format routine	Defective Write protect circuit (U11, U13)	Troubleshoot and replace defective component (see waveforms, p. 4-13)
Writes garbled data	Defective component in Erase circuit (U11, U15, U17)	Troubleshoot and replace defective component (see waveforms, p. 4-15)
	Component failure in Write circuit (U13, U15-18, U21, Q1)	Troubleshoot and replace defective component (see waveforms, p. 4-14)
	Dirty Read/Write head	Clean head with 91% Isopropyl Alcohol
Drive is always or never Write protected	Defective Write protect circuit (U11, U13)	Troubleshoot and replace defective component (see waveforms, p. 4-13)
	Defective Write protect photo sensor	Replace drive mechanism

DRIVE SELECT PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Drive select test fails	Defective select switch	Replace S2
	Defective PIA	Replace U7

DATA INTERFACE PROBLEMS		
SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
No response to commands from computer	I/O cable connections	Replace cable or tighten connections
	Command signal not getting to PIA (U7)	Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17)
	Defective PIA	Replace U7
No data output from drive to computer	I/O cable connections	Replace cable or tighten connections
	Data signal from PIA not getting to I/O connection	Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17)
	Defective PIA	Replace U7
No data input from computer to drive	I/O cable connections	Replace cable or tighten connections
	Data signal not getting to PIA (U7)	Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17)
	Defective PIA	Replace U7
Drive doesn't reboot when computer is powered down and then up again	VCC Ready signal not getting to PIA	Trace signal through (U1) and replace if necessary (see waveforms, p. 4-17)
	Defective PIA	Replace U7

If the other circuits have been checked and found good, one of the IC's in the CPU circuits is defective.

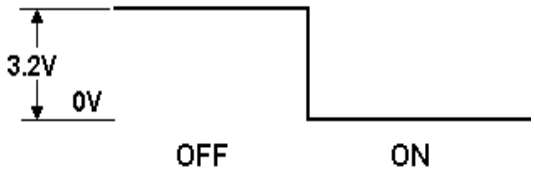
CENTRAL PROCESSING UNIT PROBLEMS	
TYPE OF FAILURE	POSSIBLE CAUSES
Power-Up failures	PIA (U7)
Boot Errors	2793, FDC (U13)
Stepper Motor failures	Microprocessor, 6507 (U9)
Drive Motor failures	Custom ROM (U10)
I/O failures	RAM, 6810 (U8)
Drive code switch not recognized	74LS04, Inverter (U16) 4MHz Crystal (Y1) 74LS74, D-type, edge-triggered flip-flop (U1) 555, Timer (U4) 74LS00, Nand gate (U6, U12)

NOTE: There is no relationship between the order of failures and possible causes.

SECTION 6

WAVEFORMS

MOTOR CONTROL SIGNALS



Pin 11 of U7

Base of Q4

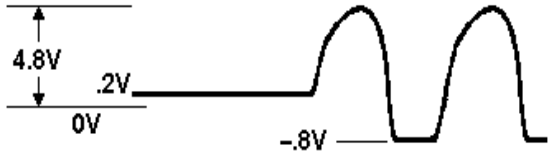
Collector of Q4

Emitter of Q4

Pin 1 at J12

The collector of Q6 is a constant 12V.

TACH FEEDBACK SIGNALS/SPEED ADJUST



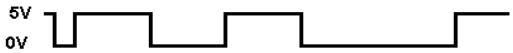
Pin 11 of U7
Schematics, Page 5-7

Pin 5 of U5
Schematics, Page 5-7

Pin 9 of U5 is a Constant 8volts.

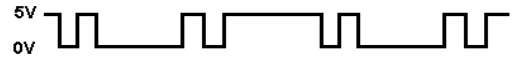
When speed pot VR2 is adjusted, the voltage on Pin 10 of U5 increases or decreases. This causes a corresponding increase or decrease in the frequency of the AC signal on the motor control lines, Pin 8 of U5 and Pins 11 and 5 of U5.

STEPPER DRIVE SIGNALS

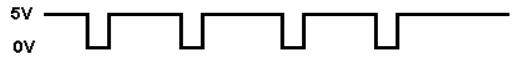


NS01

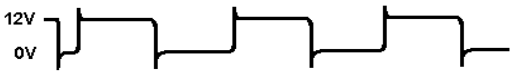
NS02



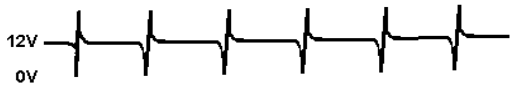
NS03



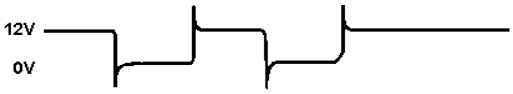
NS04



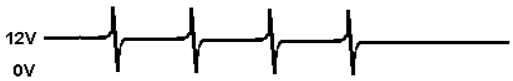
Pin 3 of U2



Pin 6 of U2



Pin 3 of U3

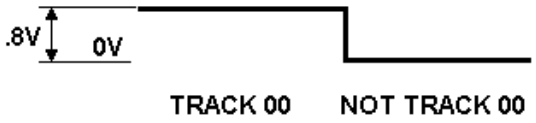


Pin 6 of U3
Pin 5 of U2 and U3 is +12V DC.

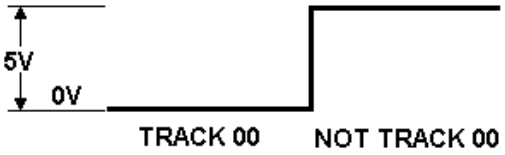
DISKETTE ENABLE SIGNAL

Enabled	Disabled
(IC U6)	(IC U6)
Pin 10 = 0V	Pin 10 = 5V
Pin 12 = 5V	Pin 12 = 0V
Pin 8 = 4.5V	Pin 8 = 4.5V

TRACK 00 SIGNAL



Base of Q5
Schematics, Page 5-7



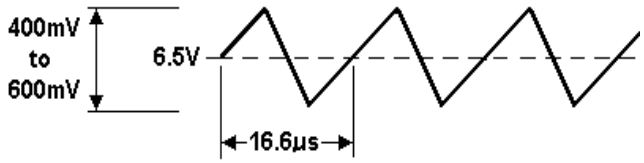
Collector of Q5
Schematics, Page 5-7

DATA - IN SIGNAL

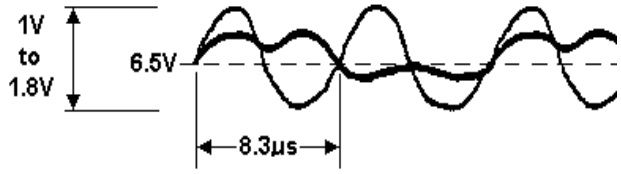
Pin 2 of U1

Pin 1 of U1

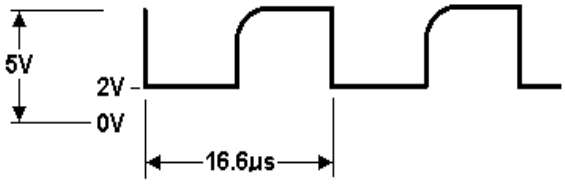
READ SIGNALS



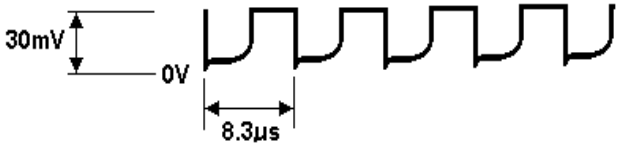
TP1 or TP2



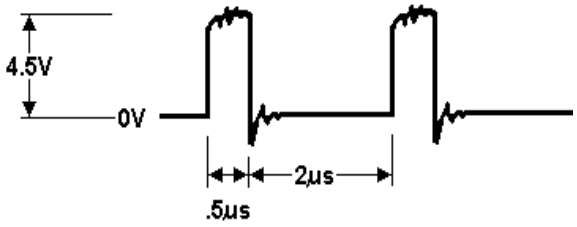
TP3 or TP4



TP5



TP16

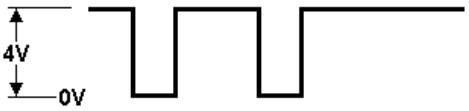


TP6

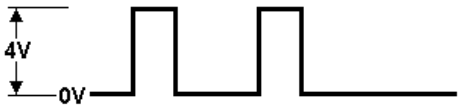
Pin 27 of U13

WRITE SIGNALS

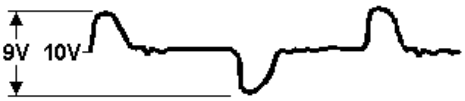
TP11



Pin 9 of U18



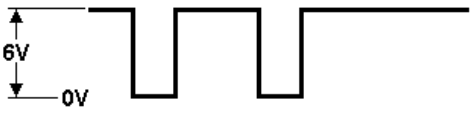
Pin 8 of U11



Pin 5 of U21

Pin 1 of U21

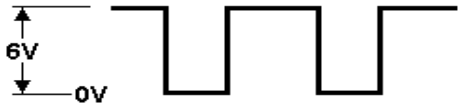
WRITE GATE SIGNALS



Pin 10 of U16

Pin 9 of U21

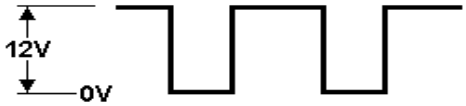
ERASE GATE SIGNAL



Pin 10 of U16

Pin 5 of U15

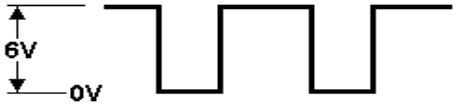
Pin 13 of U15



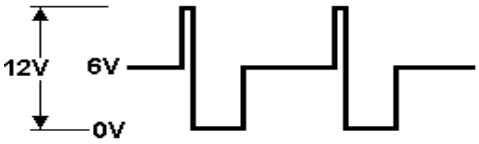
Pin 8 of U21

Collector of Q1

ERASE SIGNAL

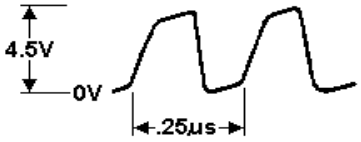


Pin 1 of U11

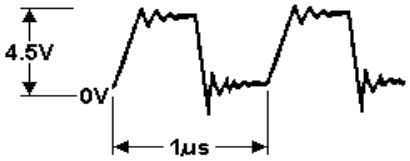


Pin 10 or 12 of U17

CLOCK SIGNALS



Pin 13 of U16
4MHz Clock



Pin 5 of U14
1MHz Clock

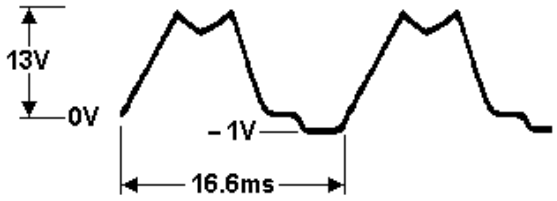
Pin 6 of U6
Phase 0 Clock

WRITE PROTECT SIGNAL

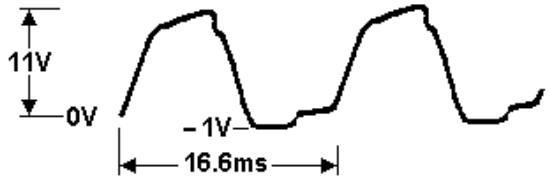
Pin 11 of U11

Pin 13 of U11

POWER SUPPLY SIGNALS (AC)

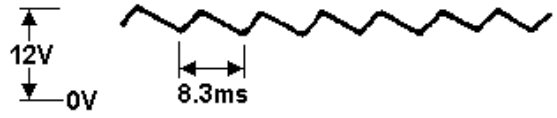


Cathode of CR20



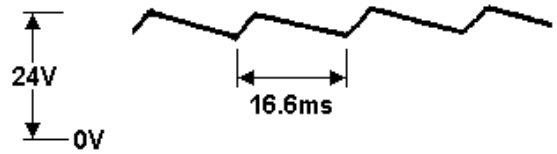
Cathode of CR20

12V



Cathode of CR20

Cathode of CR20



Cathode of CR20

Anode of CR21 = 1.7V DC

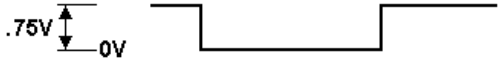
TP13 = +5V DC
TP14 = +12V DC
TP15 = GND

DATA OUT SIGNAL

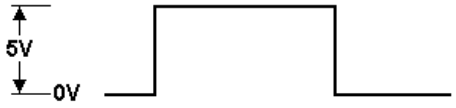
Pin 9 of U1

Pin 14 of U1

COMMAND SIGNAL

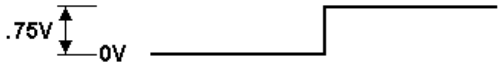


Pin 4 of U1

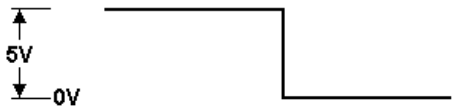


Pin 5 of U1

VCC/READY SIGNAL



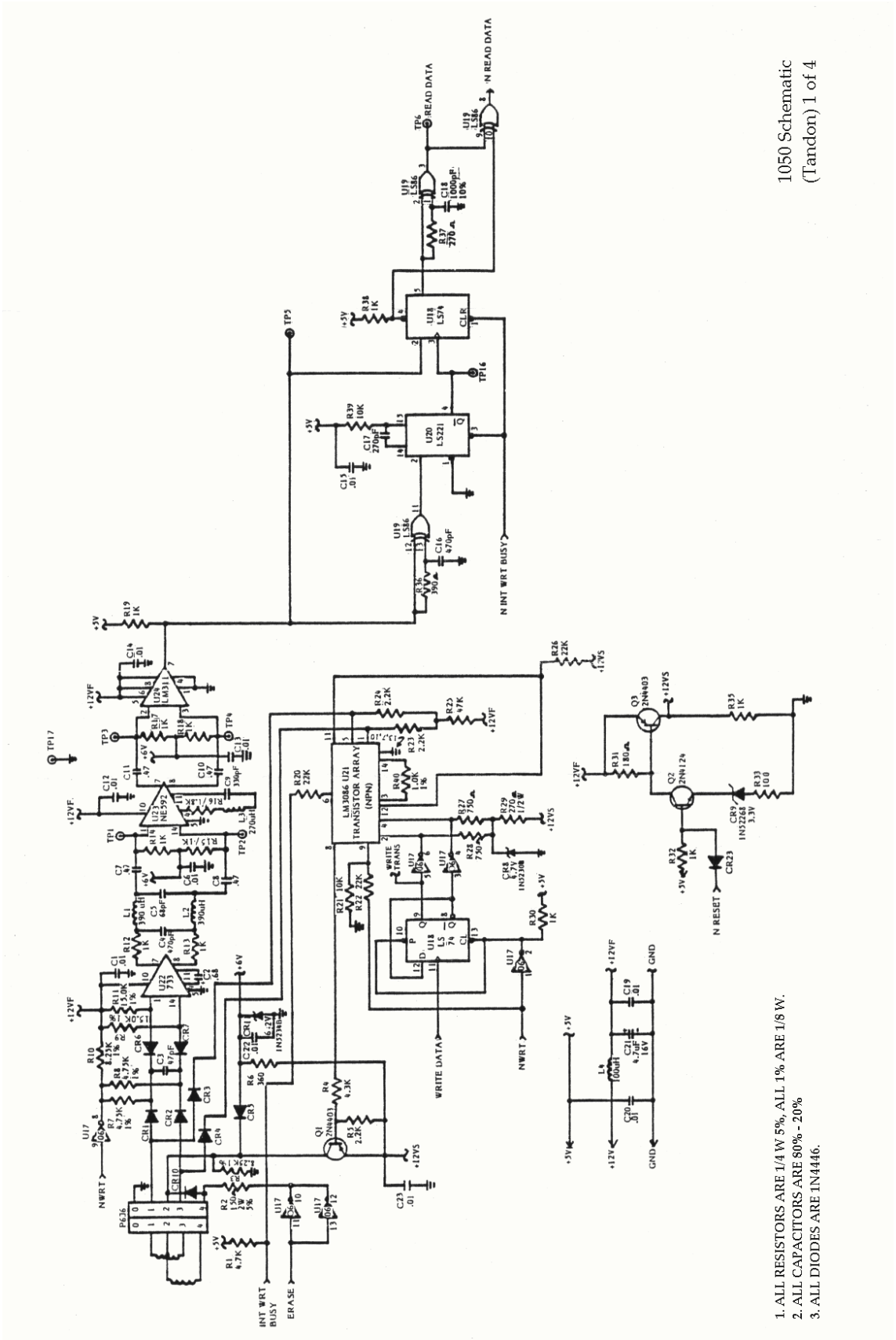
Pin 6 of U1

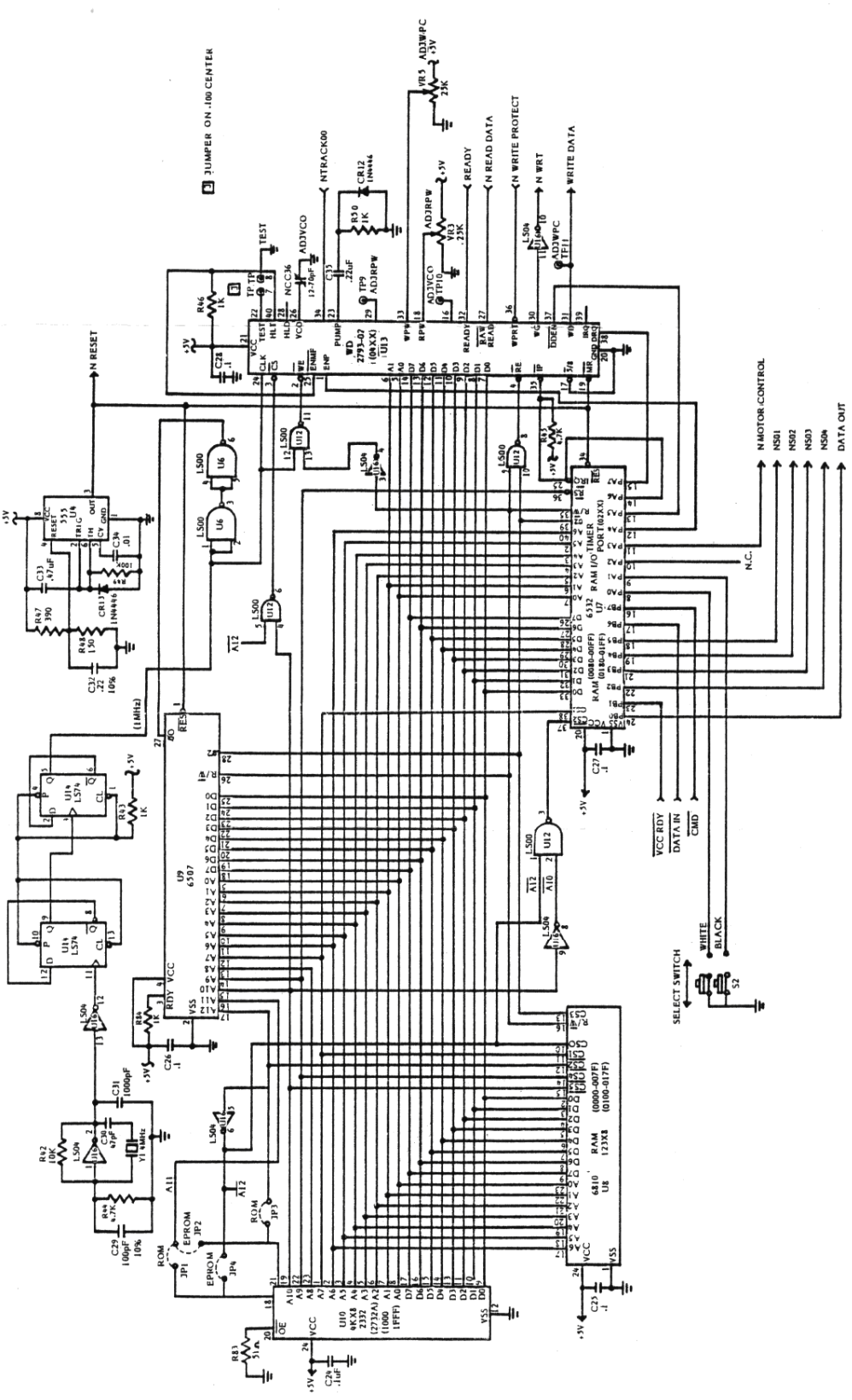


Pin 8 of U1

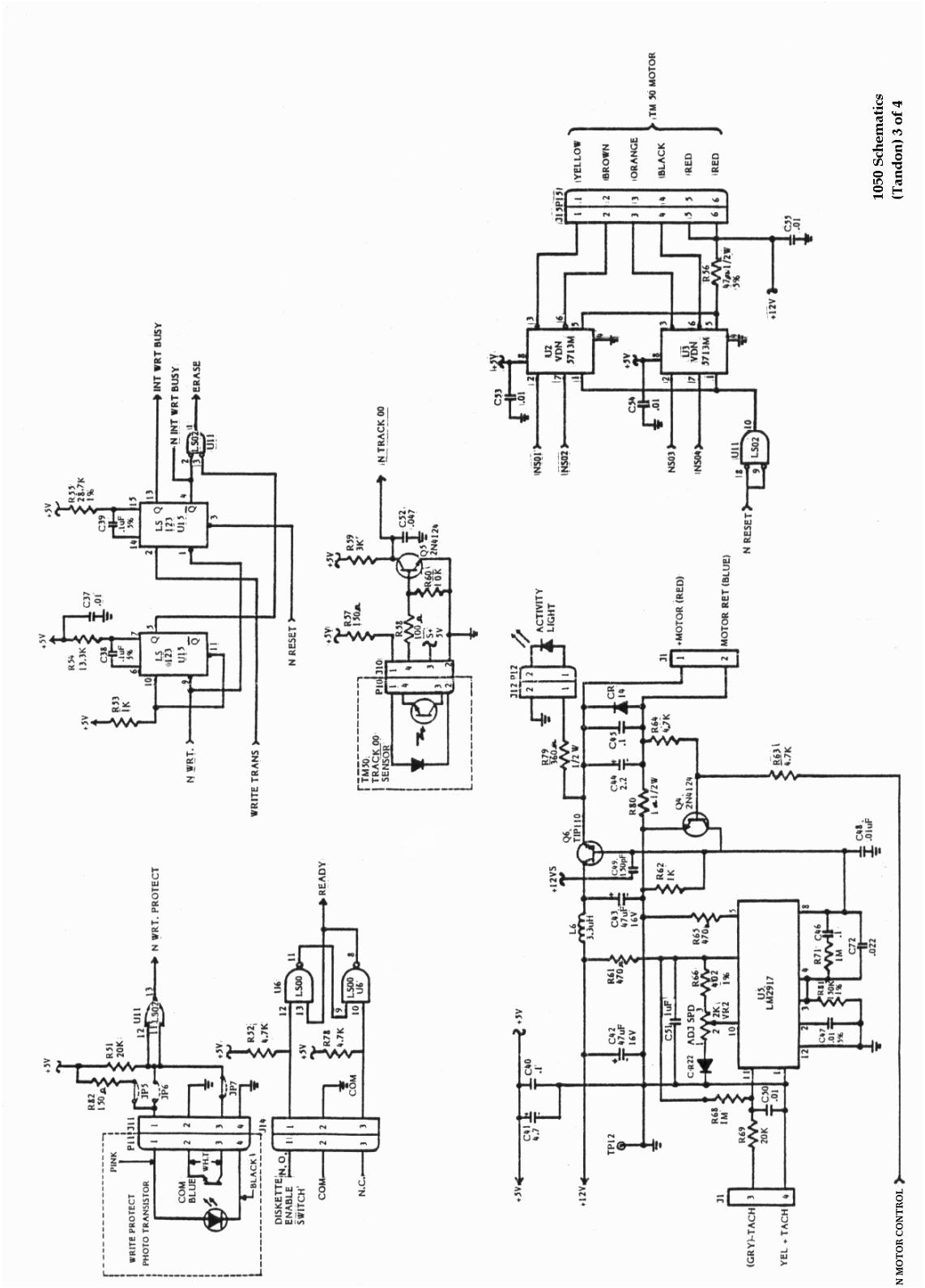
SECTION 7

SCHEMATICS AND SILKSCREENS

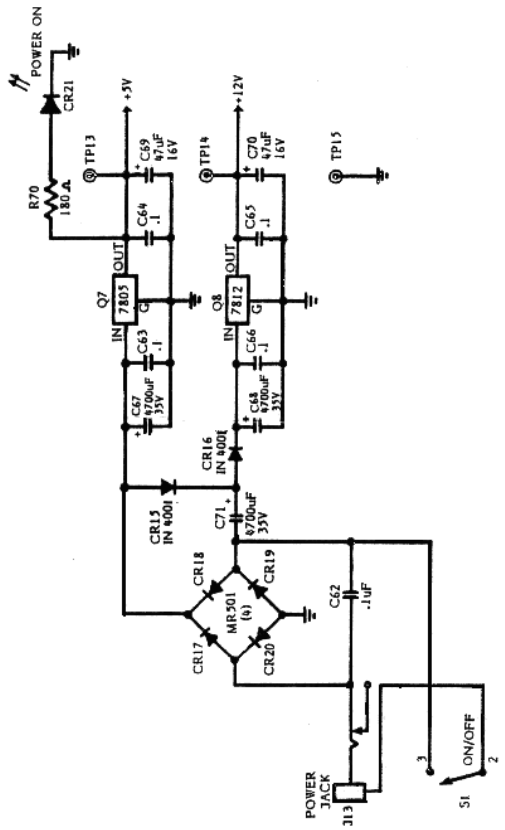

1050 Schematic
(Tandon) 1 of 4
1. ALL RESISTORS ARE 1/4 W 5%, ALL 1% ARE 1/8 W.
2. ALL CAPACITORS ARE 80% - 20%
3. ALL DIODES ARE 1N4446.

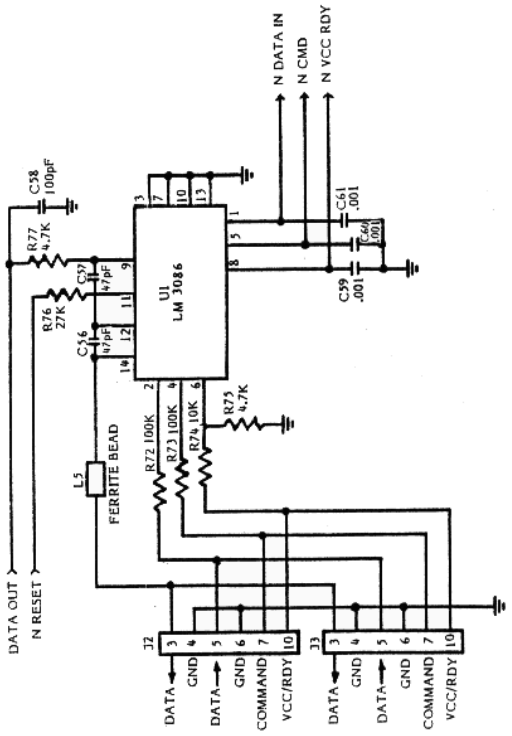


1050 Schematic
(Tandon) 2 of 4

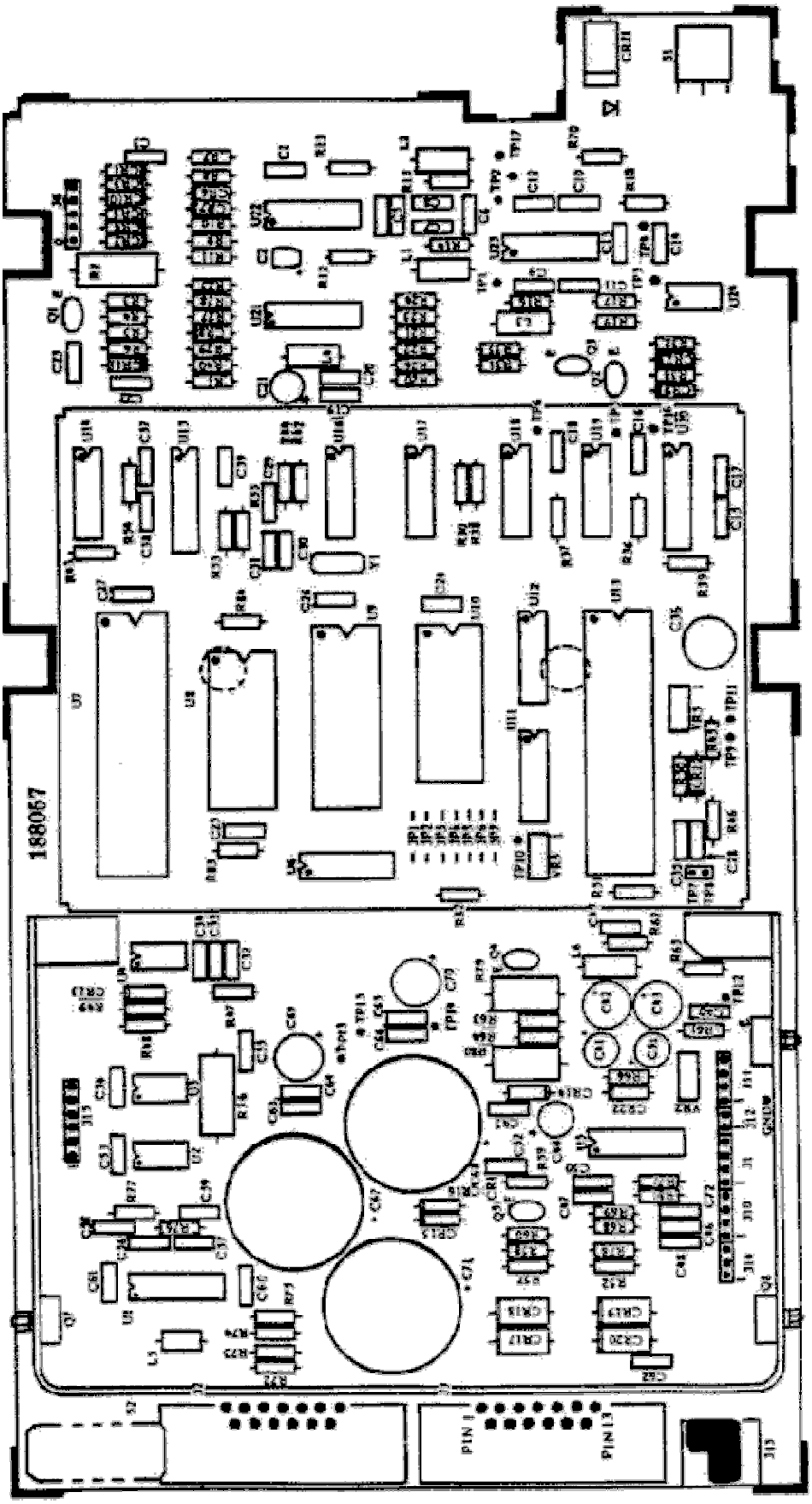


1050 Schematics
(Tandon) 3 of 4





1050 Schematics
(Tandon) 4 of 4


1050 Silkscreen
JUMPER TABLE
Write Protect - Optical
JP5
JP7
EPROM ROM
JP2
JP4
JP1
JP3
180057
PIN 1
PIN 13

SECTION 8

1050 PARTS LIST
(TANDON)

LOCATOR	DESCRIPTION	PART NUMBER
	TM 50-1 Drive Mechanism (TANDON)	FA100514
	Enclosure, Top	FC100515
	Enclosure, Bottom	FC100516
	Front Bezel	FC100517
	Photo Sensor	FC100518
	Ready Switch Assembly	FA100519
	Spindle Motor	FC100520
	1050 PCB Assembly	FA100513
L3	Inductor, 270µH	FC100521
L1, 2	Inductor, 390µH	FC100522
R2	Resistor, 150Ω, 2W	FC100524
VR2	Potentiometer, Cermet, 2kΩ	FC100525
VR3,5	Potentiometer, Cermet, 25kΩ	FC100526
Q2, 4, 5	Transistor, 2N4124	FC100527
Q1, 3	Transistor, 2N4403	FC100528
Q6	Transistor, TIP110	FC100529
CR1-7, 10, 12, 13	Diode, 1N4446 (75V/100mA switching)	FC100530
CR11	Zener diode 1N5224B, 6V2	FC100531
CR9	Zener diode 1N5226B, 3V3	FC100532
CR8	Zener diode 1N5230B, 4V7	FC100533
Y1	Crystal, 4MHz	FC100534
U15	74LS123, I.C.	FC100535
U5	LM2917, I.C.	CO17101
U2, 3	SN75478, I.C. (5713)	FC100536
C36	Capacitor Variable 12-70pF	FC100543
U22	LM733, I.C.	FC100537
U23	NE592, I.C.	CO17951
U24	LM311, I.C.	CO14332
U17	SN7406, I.C.	FC100538
U19	74LS86, I.C.	37-74LS86
U20	74LS221, I.C.	FC100540
U14, 18	74LS74, I.C.	CO16045
U1, 21	LM3086, I.C. (CA3086)	CO16821
U6, 12	74LS00, I.C.	CO14341
U11	74LS02, I.C.	CO14340
U16	74LS04, I.C.	CO17096
U4	LM555, I.C.	CO19748
U10	ROM, Custom 2732, I.C.	FC100541
U8	RAM, 6819 (1MHz), I.C.	CO14328
U9	MPU, 6507 (1MHz), I.C.	CO10745
U13	FDC, WD2793-02, I.C.	FC100542
U7	PIA, 6532 (RIOT), I.C.	CO10750
CR17, 18, 19, 20	Diode, MR501	CO14398